POWER SENSOR

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TECHNICAL FIELD OF THE INVENTION

The present invention relates to micromachined devices which are manufactured by standard foundry fabrication of complementary metal-oxide semiconductor (CMOS) integrated circuits (ICs). More particularly, the invention relates to novel micromachining of the semiconductor substrate in the vicinity of and beneath a device located on the surface of the substrate to permit device operation at significantly increased frequencies and with improved efficiencies.

BACKGROUND

With higher signal frequencies being utilized in communication systems and integrated circuits, there is a great demand for low-cost, miniature microwave components. In many applications, such components must be integrated with analog and digital circuits. Various techniques have been proposed for fabricating microwave components using micromachining techniques. These proposed techniques, however, require many photolithographic masking steps both on the top and bottom surfaces of the wafer for micromachining and metal deposition. The techniques are not compatible with commercially available CAD tools and CMOS foundry capabilities. Consequently, integration of such components with analog and digital circuits using conventional techniques is not possible.

Generally, standard CMOS silicon ICs are not suitable for integration of microwave components due to high losses in silicon at microwave frequencies. The removal of the lossy silicon substrate material in the vicinity of the metal structures, however, significantly improves the insertion loss characteristics, transmission line dispersion characteristics, phase velocity, and impedance control capability. Thus, a class of passive microwave components can be integrated into the CMOS integrated circuits. Further, the structures are fully compatible with commercial CAD tools, fabrication using commercial CMOS foundry services or the MOSIS services, and micromachined with no additional photolithographic steps.

For these reasons, it is of interest to remove the silicon substrate from directly beneath the thermal and microwave structures to improve the above-described characteristics, while still allowing the monolithic integration of CMOS electronics and overall low-cost fabrication sensors.

FIG. **1** is a cross-sectional view showing the result of an isotropic etching through one opening in a thin film layer covering a substrate. Substrate **7**, for example a silicon substrate, includes thin film **42**, opening **40**, and cavity **21**. During isotropic etching, a gaseous etchant, such as xenon difluoride (XeF_2), is typically used to create a cavity **21** directly underneath the opening **40** which propagates outward radially. Thin film **42**, covering the top of silicon substrate **7**, acts as an etch resistant mask protecting the uncovered portion of silicon substrate **7**. However, one problem that exists with this method of etching is that all cavities formed are hemispherical in shape. This places constraints on device designs that result in the prevention of fabrication of the desired device structures.

FIG. **2** is a cross-sectional view showing the result of isotropic etching through multiple openings in a thin film layer covering a substrate. Substrate **7**, for example a silicon substrate, includes thin film portions **42** and **42***a*, openings **40***a* and **40***b*, and cavities **21***a* and **21***b*. Similarly, an isotropic etchant, such as xenon difluoride (XeF_2), is used to create multiple cavities **21***a* and **21***b* directly underneath the multiple openings **40***a* and **40***b*, wherein the cavities propagate outward radially. If etching continues long enough, cavities **21***a* and **21***b* eventually merge, forming a single cavity **21** which suspends a portion **42***a* of film **42**. Thus, a device may be suspended above merged cavities **21***a* and **21***b*. One problem with this solution is that the suspended portion is limited in size. Additionally, limitations are placed on device layouts, and the bottom of the cavity is not entirely flat.

FIG. **3** is a cross-sectional view showing the result of etching using an anisotropic etchant through an opening in a masking thin film layer covering a substrate. Substrate **7**, for example a silicon substrate, includes etch resistant masking thin film **42**, opening **40**, and V-shaped cavity **21**. An anisotropic etchant, such as ethylene diamine-pyrocatechol-water (EDP), is used to create a V-shaped cavity **21** directly underneath opening **40**. The anisotropic etch follows the crystalline structure of the <100> wafer, for example, wherein side walls **21***c* and **21***d* of V-shaped cavity **21** are typically at a slope of 54.7 degrees from the surface plane (i.e. film **42**) and are aligned to the <111> crystallographic plane of substrate **7**. Similarly, a problem with this method is that the suspended portion is limited in size.

SUMMARY OF THE INVENTION

In accordance with the present invention, an apparatus and method are provided for forming a single cavity in a substrate, which may extend approximately the length of a device located on the top surface of the substrate. The present invention enables the formation of more arbitrary device structures by utilizing the advantages of isotropic and anisotropic etch processes, while mitigating their disadvantages. The cavity may be formed beneath a device having a length and a width, and may extend almost the full length of the substrate. According to the invention, after locating the device on the surface of the substrate, a first etchant is applied through one or more openings in the surface of the substrate. Subsequently, a second etchant is applied through the same opening(s) in the surface of the substrate. As a result, a single cavity is formed beneath the device, thereby suspending the device and minimizing electrical coupling.

The device may be located on the top surface of the substrate. For example, the device could be a coplanar waveguide having two ground conductors which are coplanar and spaced apart from one another, so as to extend in parallel across the substrate in the same direction. A signal conductor, which is coplanar with the ground conductors, may be located between and spaced apart from the ground conductors, to receive a power signal.

In accordance with aspects of the invention, openings are designed in the top surface of the substrate and extend in parallel along the length of the device along the outer perimeter of the ground conductors. Each of the openings is spaced apart from another such that the openings enable etching to form the single cavity beneath the device.

In accordance with other aspects of the invention, a monolithic integrated circuit assembly includes a substrate having a surface, a device with a length and a width and which may extend approximately the entire length of the substrate suspended above a cavity formed in a portion of the substrate, at least one sensor, at least a portion of which is suspended above the substrate and in proximity to a